# Project 2 - Test Case

# Parameters:

Set associativity: L1: 4, L2:8

Latency: L1: 1, L2:50, Memory:100

Address is written as this format:

(tag) (L2-L1 index) (L1 index) (offset)

Translate it into binary code by your preferred setting.

# Cache Warmup (cycle doesn’t matter)

r (001)10(00)10(00)10(x)10 1

r (002)10(00)10(00)10 (x)10 2

r (003)10(00)10(00)10 (x)10 3

r (004)10(00)10(00)10 (x)10 4

r (005)10(00)10(00)10 (x)10 5

r (006)10(00)10(00)10 (x)10 6

r (007)10(00)10(00)10 (x)10 7

r (008)10(00)10(00)10 (x)10 8

r (001)10(00)10(01)10 (x)10 9

r (002)10(00)10(01)10 (x)10 10

r (003)10(00)10(01)10 (x)10 11

r (004)10(00)10(01)10 (x)10 12

r (005)10(00)10(01)10 (x)10 13

r (006)10(00)10(01)10 (x)10 14

r (007)10(00)10(01)10 (x)10 15

r (008)10(00)10(01)10 (x)10 16

r (001)10(01)10(00)10(x)10 17

r (002)10(01)10(00)10 (x)10 18

r (003)10(01)10(00)10 (x)10 19

r (004)10(01)10(00)10 (x)10 20

r (005)10(01)10(00)10 (x)10 21

r (006)10(01)10(00)10 (x)10 22

r (007)10(01)10(00)10 (x)10 23

r (008)10(01)10(00)10 (x)10 24

r (001)10(01)10(01)10 (x)10 25

r (002)10(01)10(01)10 (x)10 26

r (003)10(01)10(01)10 (x)10 27

r (004)10(01)10(01)10 (x)10 28

r (005)10(01)10(01)10 (x)10 29

r (006)10(01)10(01)10 (x)10 30

r (007)10(01)10(01)10 (x)10 31

r (008)10(01)10(01)10 (x)10 32

L1: (5~8) (01)10 (1~2)10, L2: (1~8)(1~2)10 (1~2)10

## Case 1: Read Test - L1 Miss

Shuffle LRU

r (007)10(01)10 (01)10(x)10 10000

r (005)10(01)10 (01)10(x)10 10003

r (008)10(01)10 (01)10(x)10 10005

r (006)10(01)10 (01)10(x)10 10007

Random Read test

r (003)10(01)10 (01)10(x)10 10009 Miss

r (001)10(00)10 (01)10(x)10 10011 Miss

r (008)10(01)10 (01)10(x)10 11000 Hit

r (005)10(01)10 (01)10(x)10 11003 Miss

r (004)10(00)10 (01)10(x)10 11005. Miss

r (006)10(01)10 (01)10(x)10 12000 Miss

## Case 2: Read Test - L2 Miss (be careful about cycle)

Shuffle LRU

r (007)10(01)10 (01)10(x)10 10000

r (005)10(01)10 (01)10(x)10 10003

r (008)10(01)10 (01)10(x)10 10005

r (006)10(01)10 (01)10(x)10 10007

Random Test

r (003)10(02)10 (01)10(x)10 10100 Miss in L2

r (008)10(01)10 (01)10(x)10 10105 Hit

r (010)10(01)10 (01)10(x)10 11000 Miss in L2

r (010)10(01)10 (01)10(x)10 11000 Hit

r (011)10(00)10 (01)10(x)10 11001. Miss in L2

r (010)10(02)10 (01)10(x)10 11003. Miss in L2

r (004)10(00)10 (01)10(x)10 12000 Miss in L1

r (011)10(00)10 (01)10(x)10 12001 Hit

r (004)10(00)10 (01)10(x)10 12003 Hit

## Case 3: Write Test, L1 Miss, L2 Hit

Write Hit

w (007)10(01)10 (01)10(x)10 10000

r (005)10(01)10 (01)10(x)10 10003

w (008)10(01)10 (01)10(x)10 10005

r (006)10(01)10 (01)10(x)10 10007

Write Miss in L1 but Hit in L2

w (007)10(00)10 (01)10(x)10 10100. Miss in L1

eviction (007)10(01)10 (01)10(x)10

r (004)10(01)10 (01)10(x)10 10103. Miss in L1

w (007)10(01)10 (01)10(x)10 11000. Miss in L1

eviction (008)10(01)10 (01)10(x)10

r (001)10(00)10 (01)10(x)10 11003 Miss in L1

w (007)10(01)10 (01)10(x)10 11005. Hit

r (005)10(01)10 (01)10(x)10 12003 Miss in L1

eviction (007)10(00)10 (01)10(x)10

w (002)10(00)10 (01)10(x)10 12005. Miss in L1

r (007)10(01)10 (01)10(x)10 12007. Hit

## Case 4: Write Test, L1 Miss, L2 Miss

Write Hit

w (007)10(01)10 (01)10(x)10 10000

r (005)10(01)10 (01)10(x)10 10003

w (008)10(01)10 (01)10(x)10 10005

r (006)10(01)10 (01)10(x)10 10007

Write Miss in L1 and L2

w (010)10(01)10 (01)10(x)10 10100. Miss in L2

eviction (007)10(01)10 (01)10(x)10

r (005)10(02)10 (01)10(x)10 10103. Miss in L2

w (009)10(01)10 (01)10(x)10 11000. Miss in L2

eviction (008)10(01)10 (01)10(x)10

r (005)10(02)10 (01)10(x)10 11003 Hit

r (010)10(01)10 (01)10(x)10 11005. Hit

r (001)10(01)10 (01)10(x)10 11007. Miss in L2

w (010)10(01)10 (01)10(x)10 12003. Hit

w (010)10(02)10 (01)10(x)10 12005. Miss in L2

eviction (009)10(01)10 (01)10(x)10

w (009)10(01)10 (01)10(x)10 12007. Miss in L1

r (010)10(02)10 (01)10(x)10 13003. Hit